FLEX SWITCH™

(Simple Off-Line/PFC & >9V DC/DC Switcher)

Features

- Drive one or hundreds of LEDs including White LEDs
- Programmable Current Source (mA to A)
- Programmable Voltage Source (Steps Up or Down)
- Integrator Lock Loop Technology (IL^2)
  - Built in Soft Start
  - Allows Discontinuous Feedback
  - Eliminates Compensation Components
  - Eliminates Output Averaging Filters
  - Inherent Dither to Reduce EMI
- Eliminates High Voltage Input Electrolytic Capacitor
- Smallest and Most Reliable Off-Line Solution
- Isolated or Non-Isolated Applications
- Can be Operated Directly from Rectified AC Mains
- 10V to 400V Input Range Internal Regulator
- <1.5mA Operating Supply Current
- Programmable Feed Forward Regulation
- Programmable Feedback Sense Threshold (mV to V)
- Integrating Differential Sense Feedback

Applications

- LED driver
- Power Factor Correction
- Constant Current or Voltage Source
- Battery Charger / PWM Housekeeping Supplies
- Traffic Lights / Street Lights
- Back Lighting of Flat Panel Displays
- Advertising Signs

General Description

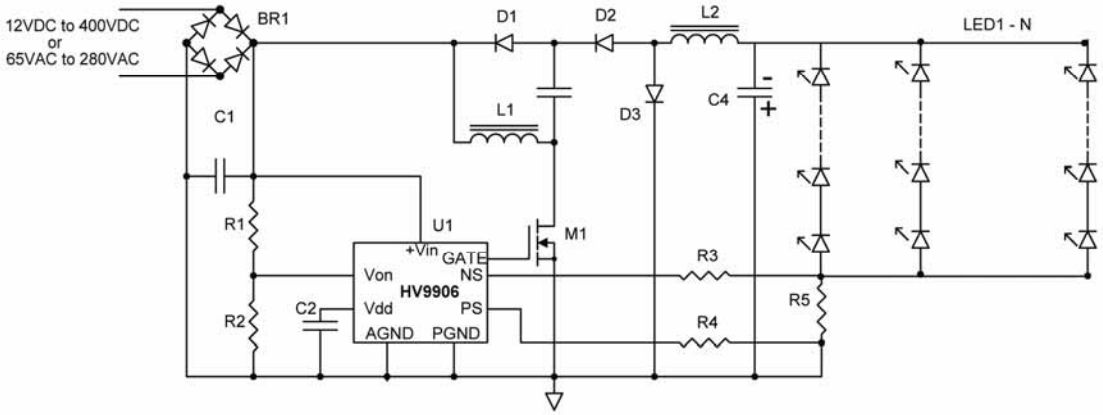
The Supertex HV9906 allows the development of the smallest possible, most reliable, offline and wide DC/DC conversion range converters for driving LEDs and other applications. The HV9906 combines internally all the components required to operate directly from the rectified AC line with a feedback mechanism that eliminates compensation components.

The HV9906 is capable of driving cascaded converters (multi-converters), which have been shown to provide the best performance to component count trade off for wide conversion range applications like off-line converters with or without power factor correction (PFC). Bulky and unreliable electrolytic capacitors can be replaced with lower value non-electrolytic ones or eliminated completely when using HV9906.

Proper choice of external components will allow the programming of currents from <1mA to several amps.

The HV9906 utilizes a programmable inversely proportional fast feed forward algorithm to calculate output on time and a novel Integrating Lock Loop (IL^2) feedback with programmable threshold differential sensing. The sensed feedback may be positive or negative with respect to ground and the signal may be discontinuous. This algorithm when used with certain multi-converters such as the flyback-buck, with a fixed load, results in near constant frequency with only a small dither which helps meet FCC requirements.

Typical Application Circuit



Supertex, Inc. 1235 Bordeaux Drive, Sunnyvale, CA 94089 TEL: (408) 222-8888 FAX: (408) 222-4895 www.supertex.com

Absolute Maximum Ratings*

$+V_{IN}$ Input Voltage	-0.3V to +450V
V_{DD}	-0.3V to +15V
V_{ON} Pulse Width Control Voltage	-0.3 to +10V
PS & NS Pin Feedback Voltage	-0.3V to +10V
Operating Ambient Temperature Range	-40°C to +85°C
Operating Junction Temperature Range	-40°C to +150°C
Storage Temperature Range	-65°C to +150°C
Thermal Resistance Junction to Ambient, SOIC	159°C/W
Thermal Resistance Junction to Case, SOIC	45°C/W
Thermal Resistance Junction to Ambient, Plastic DIP	110°C/W
Thermal Resistance Junction to Case, Plastic DIP	35°C/W

*All voltages referenced to AGND and PGND connected together.

Ordering Information

Package Options	
8 Pin Plastic DIP	8 Pin SOIC
HV9906P	HV9906LG

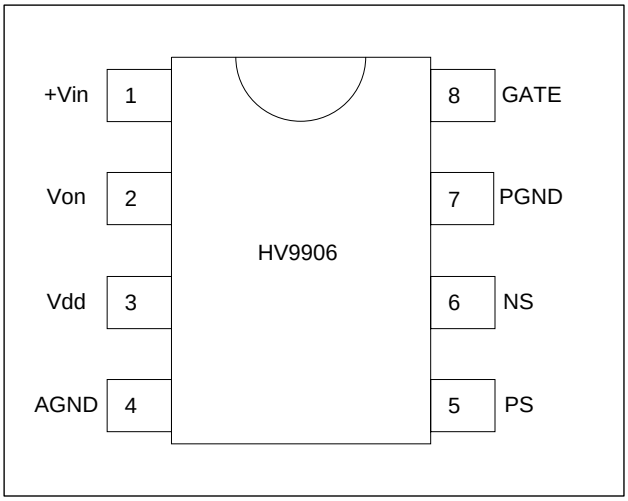
Electrical Characteristics *(Unless otherwise noted T_A = 25°C)*

Symbol	Parameter	Min	Typ	Max	Units	T_A	Conditions
Input Regulator/Vdd Supply							
$+V_{IN}$	Input Voltage	12		400	V	*	Typical under UVLO
$+I_{IN}$	Input Current			1.5	mA	*	Gate pin open and operating at F_{MAX}
$V_{DD(REG)}$	Internal Regulator Output Voltage		10	11.5	V	*	V_{IN} = 12V
$V_{DD(REG)}$	Internal Regulator Output Voltage		10	12.5	V	*	V_{IN} = 400V
V_{UVLO}	Under Voltage Lockout Threshold		8.0		V		Decaying V_{DD}
V_{HYST}	Under Voltage Lockout Hysteresis		0.50		V		
MOSFET Gate Drive Output							
t_R	Rise Time			75	nSec		C_{GATE} = 750pF
t_F	Fall Time			75	nSec		C_{GATE} = 750pF
PWM							
$P(V_{ON})$	Output Pulse Width at V_{ON}		215	300	nSec		V_{ON} = 5.0V
$P(V_{ON})$	Output Pulse Width at V_{ON}	2	3.35		uSec		V_{ON} = 0.2V
P_{MAX}	Maximum Output Pulse Width		17.8		uSec		V_{ON} = 0V
f_{MIN}	Minimum Output Frequency	10	13.5	17	KHz		
f_{MAX}	Maximum Output Frequency	250		450	KHz		
Current Sense							
V_{PS}	Positive Sense Pin Voltage	0.9	1	1.1	V	*	Note: V_{PS} and V_{NS} are matched
V_{NS}	Negative Sense Pin Voltage	0.9	1	1.1	V	*	Note: V_{PS} and V_{NS} are matched
Pulse Width Control Feed Forward Voltage							
V_{ON}	Effective Pulse Width Control Voltage Range	0.2		6.0	V	*	

The "*" denotes specifications that apply over the full temperature range (-40°C to +85°C)

Supertex, Inc. 1235 Bordeaux Drive, Sunnyvale, CA 94089 TEL: (408) 222-8888 FAX: (408) 222-4895 www.supertex.com

Pinout



Pin Description

$+V_{IN}$ – This pin is the input to the internal linear regulator.

V_{ON} –The voltage applied to this pin by a resistor voltage divider from $+V_{IN}$ controls the on time (pulse width) of the gate output.

V_{DD} – This pin is the output of the internal linear regulator and the supply pin for the internal circuits. It must be bypassed with a low ESR capacitor to provide a low impedance path for the gate drive and be capable of storing sufficient energy so that the voltage does not decay below the UVLO threshold during the time when the input voltage is below the minimum required by the regulator.

AGND – This pin is the common connection for analog circuits.

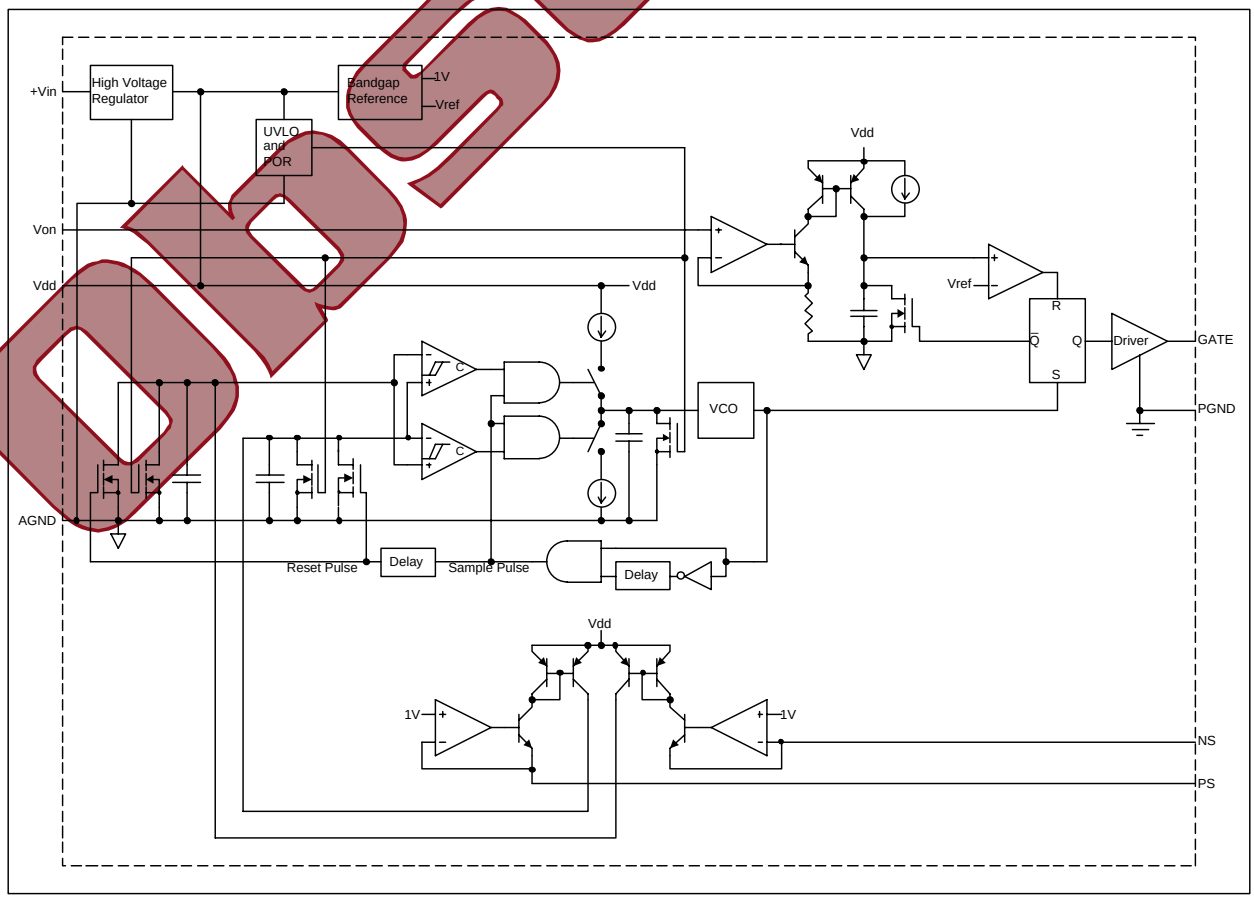
GATE – This pin is the output for driving the gate of an external N-channel MOSFET.

PGND – This is the common connection for the GATE drive circuit.

NS – This pin is the negative terminal of the differential sense feedback circuit.

PS – This pin is the positive terminal of the differential sense feedback circuit.

Functional Block Diagram



Supertex, Inc. 1235 Bordeaux Drive, Sunnyvale, CA 94089 TEL: (408) 222-8888 FAX: (408) 222-4895 www.supertex.com

Functional Description

The HV9906 consists of the following functional blocks:

- High Voltage Regulator
- Bandgap Reference
- Under Voltage Lockout and Power On Reset
- Voltage Controlled Oscillator
- Feed Forward On Time Control
- Differential Sense Circuit and Programmable Reference
- Integrator
- Sample and Hold VCO Control
- Gate Driver
- Soft Start

The following sections provide a detailed explanation of each of these blocks.

High Voltage Regulator

All internal circuits operate from a nominal 10V V_{DD} supply provided by an onboard linear regulator capable of accepting input voltages up to 400V. This regulator blocks reverse current flow from V_{DD} to $+V_{IN}$, such as in the case when the input voltage is a full wave rectified sine wave. Therefore, if a sufficiently large bypass capacitor (>1μF) is connected to V_{DD}, the operation of the circuit can be maintained during the times when the full wave rectified input voltage is less than the regulated output voltage. High operating frequency and high input voltage applications will result in increased power dissipation in the regulator. For these applications efficiency may be improved by bootstrapping the V_{DD} pin if a non-isolated +10V output is available. Supertex's high voltage technology allows a very low current regulator, rather than a shunt, to power the IC. This makes it possible to continuously operate the IC from the AC line, within thermal limits & without bootstrapping, in certain applications.

Bandgap Reference

As the regulator turns on and the V_{DD} voltage rises, a bandgap reference is activated to establish the regulation point of the regulator and provide the required references for the internal circuits. The references are strictly internal and not available at any pin of the device.

Under Voltage Lockout and Power On Reset

On initial power application the high input voltage (up to 400V) linear regulator charges the capacitor connected to V_{DD} and seeks to provide a stable supply for the internal circuitry. Under voltage lockout (UVLO) holds the voltage controlled oscillator (VCO) disabled until the V_{DD} supply rises above a nominal 8.5V and power on reset (POR) clamps the capacitors in the sample and hold and integrator circuits low for a short time thereafter, thus setting the VCO to its lowest frequency state. The UVLO has a 0.5V hysteresis to prevent false triggering due to ripple on V_{DD}.

Voltage Controlled Oscillator

The period of the voltage controlled oscillator (VCO) is determined by the output of the sample and hold circuit while the feed forward control from the V_{ON} pin provides fast direct control of the oscillator output on time. For unusual operating circumstance the VCO may be driven to its maximum frequency and the on time may exceed the period of the oscillator. This will cause cycle skipping or an effective reduction in output frequency by an integer factor.

Feed Forward On Time Control

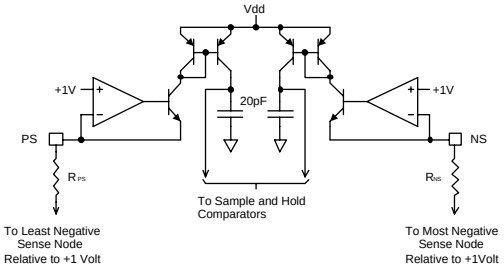
The output signal to the gate driver is controlled by a latch that is set by the output of the VCO and reset by the feed forward on time control, thus the voltage applied to the V_{ON} pin provides direct and continuous control of the gate drive on time. The on time is inversely proportional to the applied voltage and there is an internally set limit to the maximum on time (17.8μS) so that 0V will not result in an infinite on time. Refer to "Programming On Time" in the Design Information section.

To operate in discontinuous conduction mode with constant energy transfer per cycle a resistor divider from the input voltage is connected to the V_{ON} pin, thereby providing fast feed forward input regulation control. This control loop can easily track a rectified sine wave of input voltage at 50Hz, 60Hz or 400Hz provided that the capacitor connected at V_{DD} can store sufficient energy to prevent decay below the UVLO threshold during the time when the rectified sine wave input voltage at $+V_{IN}$ is below 10V. For a 100V 50Hz rectified sine wave a 3.3μF capacitor connected to V_{DD} is sufficient to guarantee stable operation.

For power factor correction applications an input voltage peak detector or a low pass filter can be used to drive the V_{ON} pin. This will provide an essentially constant on time control voltage resulting in an energy transfer per oscillator cycle directly proportional to the input voltage.

Differential Sense Circuit and Programmable Reference

The following simplified equivalent circuit is provided to clarify the operation and programming of this circuit.



This differential sense circuit is typically used to monitor the output voltage or current of a power converter. The circuit operates by sourcing current (typically 5μA) from both the PS and NS pins which are regulated at a nominal +1V and the control loop seeks to maintain a sense node voltage (voltage across a current sense resistor or the voltage across a resistor divider) that will make the NS and PS currents equal. Regulation is established when there is zero current difference in the PS and NS pins. This differential common mode sense method reduces noise sensitivity and enables the user to define the magnitude of the sensed voltage (i.e. +100mV for high efficiency or –2.5V to escape the noise floor) and thus the effective reference, provided the sensed nodes are at less than +1V with respect to ground.

To ensure tight regulation, 10nF ceramic or film capacitors are needed from PS and NS to ground, respectively. These capacitors ensure a matched slew rate from supply to supply and further provide a dominant pole compensation of both transconductors.

Supertex, Inc. 1235 Bordeaux Drive, Sunnyvale, CA 94089 TEL: (408) 222-8888 FAX: (408) 222-4895 www.supertex.com

Functional Description - *continued*

The voltage difference between the sensed nodes will require the selection of resistor values in series with the NS and PS pins that will result in current balance. While balance can be achieved even if neither sensed node is at ground potential, care must be taken to assure that the dynamic voltage excursions of the sensed node within the design operating range (i.e. 50KHz to 250KHz) of the particular application does not result in common mode current swings in the PS and NS pins that would result in saturation of the integrators. Saturation at frequencies below the minimum operating frequency of the application is permitted* since by design the circuit will soft start from its lowest frequency.

To regulate on a sense node voltage of +0.5V with respect to ground connect a 200kΩ resistor from the NS pin to the ground end of the sense element and a 100kΩ resistor from the PS pin to the +0.5V end of the sense element. Since the voltage drop on the 200kΩ resistor connected to the NS pin is 1V, a reference current of 5μA is established. To achieve current balance in the PS pin the sensed node must rise to +0.5V.

For regulating a sense node voltage of –1V with respect to ground connect a 200kΩ resistor from the PS pin to the ground end of the sense element and a 400kΩ resistor from the NS pin to the –1V end of the sense element. Since the voltage drop on the 200kΩ resistor connected to the PS pin is 1V, a reference current of 5μA is established. To achieve current balance in the NS pin the sensed node must fall to -1V.

For calculating the required resistor values refer to “Programming the Sense Inputs” in the Design Information section.

Integrator

The differential output current of the differential sense circuit is fed to two matched internal 20pF capacitors that make up the differential integrator circuit. The tolerances of these integrated capacitors are typically ±5%, however, since they are matched, their absolute values only affect the peak voltage of the integrators. Operating at the lowest frequency results in the highest peak voltage on the integrators, which will saturate if the peak voltage on the capacitors exceeds 6V, resulting in a loss of regulation. This must be taken into consideration when deciding on the value of the sense currents in the PS and NS pins. The signals at the sensed nodes may be discontinuous (i.e. controlling the average output current into LEDs) since the signals are cycle-averaged by the differential integrator. The differential output of the integrator is fed to the sample and hold comparators.

*The circuit soft starts from the lowest frequency, therefore it is very likely that the integrators will saturate during startup. By design the VCO frequency will be incremented in the event of a saturated condition, thereby guaranteeing that the circuit will start.

Sample and Hold VCO Control

The cycle-averaged outputs of the differential integrator are compared by the window comparator of the sample and hold circuit. If the differential integrator outputs are unequal the sample and hold circuit increments or decrements the VCO control voltage by a fixed small step resulting in a shorter or longer subsequent VCO cycle and thus an increased or decreased frequency. When the cycle-averaged signals from the differential integrator are nearly equal (within the hysteresis band of the comparators) the sample and hold function is halted and the off time is unchanged. Since the frequency is incremented or decremented in small fixed steps at the end of each cycle the rate of frequency increase or decrease is a function of the frequency and thus the oscillator frequency will change exponentially.

In this manner the Integrator Lock Loop (IL^2) feedback controls the oscillator frequency based on a cycle-averaged sensed value to maintain output regulation. For certain off-line topologies, the result is near fixed frequency operation for a fixed load with a dither of a few KHz which helps in meeting FCC conducted emission requirements.

Gate Driver

The gate driver buffers the output of the VCO and provides sufficient gate drive power to achieve rise and fall times below 75nS into a 750pF equivalent MOSFET gate. The under voltage lockout (UVLO) assures that sufficient voltage is available to drive the gate of standard or logic level threshold MOSFETs.

Soft Start

On initial power application the UVLO and POR resets the output latch and sets the VCO to its lowest frequency state, which represents minimum power transfer per VCO cycle. Thereafter, the differential sense feedback loop increments the frequency in small steps, increasing the power transfer rate until output regulation is achieved, thereby providing the required soft start function.

Supertex, Inc. 1235 Bordeaux Drive, Sunnyvale, CA 94089 TEL: (408) 222-8888 FAX: (408) 222-4895 www.supertex.com

Design Information

Programming On Time

The instantaneous voltage applied to the V_{ON} pin determines the gate drive output on time for the VCO cycle. The on time is inversely proportional to the voltage applied to the V_{ON} pin and may be calculated using the following equation:

$$T_{ON} \approx \left[0.085 + \frac{0.65}{V_{ON}}\right] \times 10^{-6}$$

Where the effective control range of V_{ON} is limited between 0.2V and 6V. For V_{ON} = 0V P(V_{ON}) defaults to a nominal maximum of 17.8µS.

Depending on the converter topology and worst case operating conditions the minimum on time and thus the duty cycle may be programmed.

Programming the Sense Inputs

The PS and NS sense pins are regulated at +1V and each needs to be programmed to source the same current at the converter output regulation set point.

In order to calculate the values of R_{NS} and $R_{PS,}$ the maximum sense current, which will avoid integrator saturation, must be determined. Since by design the circuit will inherently soft start from its lowest frequency, the designer only needs to establish the lowest operating frequency (f_{MIN}) for the design, which corresponds to minimum converter output power under closed loop control. Once this frequency is established the maximum PS pin sense current $I_{PS(MAX)}$, which occurs during start up when V_{PSENSE} = V_{NSENSE}, can be calculated using the following equation.

$$I_{PS(MAX)} = C_{MIN} \times V_{SAT} \times f_{MIN}$$

Where C_{MIN} is the minimum value of the integrator capacitors, V_{SAT} is the minimum saturation level of the integrators and f_{MIN} is the minimum operating frequency of the converter. Inserting these values the above equation can be simplified.

$$I_{PS(MAX)} = (0.95) \times (20 \times 10^{-12}) \times 6 \times f_{MIN}$$

$$I_{PS(MAX)} = 1.14 \times 10^{-10} \times f_{MIN}$$

For the general case, where at regulation neither sensed node might be at ground potential, the following equation may be used to calculate the required R_{PS} resistor value where $V_{PSENSE(MIN)}$ is the most negative value that the node will see during starting or normal operation.

$$R_{PS} = \frac{1V - V_{PSENSE(MIN)}}{I_{PS(MAX)}}$$

Once the value of R_{PS} has been determined the I_{PS} and I_{NS} sense currents at the regulation point can be calculated and the value of R_{NS} can be determined as follows.

$$I_{PS} = I_{NS}$$

$$R_{NS} = \frac{1V - V_{NSENSE}}{I_{NS}}$$

Where I_{NS} = I_{PS} = average current in the NS and PS pins at stable output regulation, V_{NSENSE} is the most negative sensed node voltage with respect to +1V and V_{PSENSE} is the least negative sensed node voltage with respect +1V. V_{NSENSE} and V_{PSENSE} must be less than +1V and V_{NSENSE} is always more negative than V_{PSENSE}.

Example 1.

For a converter operating at a minimum frequency of 50KHz and sensing a –1V feedback node voltage with respect to ground, the resistors connected in series with the PS and NS pins will be determined as follows.

$$I_{PS(MAX)} = 1.14 \times 10^{-10} \times 5 \times 10^{4} = 5.7\mu A$$

To provide a margin of safety let $I_{PS(MAX)}$ = 5µA. Since in this configuration the resistor in series with the PS pin is connected to ground, the sense node voltage $V_{PSENSE(MIN)}$ = 0V.

$$R_{PS} = \frac{1V - V_{PSENSE(MIN)}}{I_{PS(MAX)}} = \frac{1-(0)}{5 \times 10^{-6}} = 200k\Omega$$

$$R_{NS} = \frac{1V - V_{NSENSE}}{I_{NS}} = \frac{1-(-1)}{5 \times 10^{-6}} = 400k\Omega$$

Example 2.

For a converter operating at a minimum frequency of 100KHz and sensing a +0.5V feedback node voltage with respect to ground, the resistors connected in series with the PS and NS pins will be determined as follows.

$$I_{PS(MAX)} = 1.14 \times 10^{-10} \times 1 \times 10^{5} = 11.4\mu A$$

To provide a margin of safety let $I_{PS(MAX)}$ = 10µA. In this configuration the most negative value of $V_{PSENSE(MIN)}$ occurs during startup at which time it is 0V.

$$R_{PS} = \frac{1V - V_{PSENSE(MIN)}}{I_{PS(MAX)}} = \frac{1-(+0.5)}{10 \times 10^{-6}} = 50k\Omega$$

$$R_{NS} = \frac{1V - V_{NSENSE}}{I_{NS}} = \frac{1-0}{10 \times 10^{-6}} = 100k\Omega$$

Protection

The HV9906 used as a current source is inherently protected in the case of an output short. Over voltage protection is easily accomplished, in the flyback-buck application for example, with no more than two diodes. Simple protection for voltage mode applications, and other topologies is easy to accomplish. Call for more information.

Supertex, Inc. 1235 Bordeaux Drive, Sunnyvale, CA 94089 TEL: (408) 222-8888 FAX: (408) 222-4895 www.supertex.com

Design Information - *continued*

Managing Power Dissipation

The maximum I_{DD} current required is the sum of the chip operating current plus the current required to drive the gate of the external MOSFET at the maximum operating frequency of the particular application. Depending on the available data on the MOSFET the current can be calculated by one of the following methods.

$$I_{GATE} = f \times Q_{GATE}$$

or

$$I_{GATE} = f \times C_{GATE} \times V_{GATE}$$

Where f is the maximum operating frequency for the application, Q_{GATE} is the total gate charge, C_{GATE} is the effective gate capacitance and V_{GATE} is the maximum gate drive voltage, which is approximately equal to V_{DD}.

The input regulator supplies all the current and the worst-case total regulator current may be calculated as follows.

$$I_{IN} = 1.5 \times 10^{-3} + I_{GATE} = 1.5 \times 10^{-3} + f \times Q_{GATE}$$

or

$$I_{IN} = 1.5 \times 10^{-3} + I_{GATE} = 1.5 \times 10^{-3} + f \times C_{GATE} \times V_{GATE}$$

As an example for a particular application where C_{GATE} = 750pF and the maximum operating frequency is f = 200KHz the regulator input current

$$I_{IN} = 1.5 \times 10^{-3} + 200 \times 10^{3} \times 750 \times 10^{-12} \times 10 = 3mA$$

If the application is operating in an open-air environment with a known maximum ambient temperature, then the maximum allowable input voltage may be calculated using the following equation.

$$V_{IN(max)} = \frac{T_j - T_a}{R_{\theta ja} \times I_{IN}}$$

Where T_j is the maximum operating junction temperature, T_a is the maximum ambient temperature, $R_{\theta ja}$ is the thermal resistance for the particular package from junction to ambient and I_{IN} is the required input current.

Using the I_{IN} calculated in the previous example in a 50°C maximum ambient and a plastic DIP package the maximum allowable input voltage is as follows.

$$V_{IN(max)} = \frac{150 - 50}{110 \times 3 \times 10^{-3}} = 303V \quad \text{DC or RMS}$$

In the event that this maximum allowable input voltage is less than what is required by the application, then the following means may be considered to reduce the dissipation in the regulator.

1. Bootstrapping V_{DD} from an output of the converter
2. If the input is DC then a resistor can be added in series with V_{IN}
3. If the input is AC then a depletion MOSFET may be added in series with V_{IN}
4. Encapsulating the circuit with a high thermal conductivity material
5. Boostrapping V_{DD} from an auxiliary bifilar inductor winding or from an auxiliary transformer winding.

Bootstrapping V_{DD}

Forcing V_{DD} to a voltage greater than the regulation set point voltage of the internal regulator (i.e. 13V) will force the regulator to turn off and all the required operating current will be provided by the forcing source of power. If this power source is derived from the output of the converter, possibly by means of a secondary winding on one of the inductors or an additional winding on a transformer, then the internal regulator will provide the required current during startup only. Care must be taken to assure that the absolute maximum voltage rating of the V_{DD} pin is not exceeded.

After initial startup, bootstrapping will reduce the power dissipated, even at the absolute maximum V_{DD} voltage, to an essentially negligible level ($V_{DD(max)}$ x I_{IN} =15V x 3mA = 45mW).

Operating from a DC input

For DC applications there is usually some minimum operating voltage. A resistor may be added in series with $+V_{IN}$ which can reduce the effective input voltage to $+V_{IN(min)}$, thereby transferring some of the power dissipation to the series resistor.

Using the input current of 3mA previously calculated and assuming an operating input voltage range (V_S) of 100VDC to 250VDC for the application, the maximum value of the series resistor can be calculated as follows.

$$R_{series} = \frac{V_{S(min)} - V_{IN(min)}}{I_{IN}} = \frac{100 - 10}{3 \times 10^{-3}} = 30k\Omega$$

The maximum power dissipation in the resistor will be

$$W_R = R_{series} \times I_{IN}^2 = 30 \times 10^3 \times (3 \times 10^{-3})^2 = 0.27W$$

and the maximum power dissipation in the HV9906 will be

$$W_{IC} = V_{IN(max)} \times I_{IN} - W_R = 250 \times 3 \times 10^{-3} - 0.27 = 0.48W$$

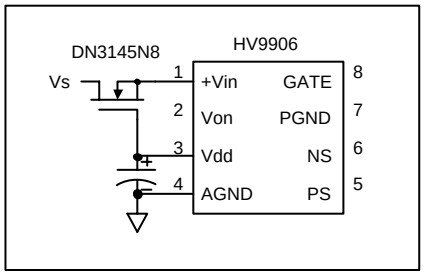
which for an SOIC packaged device will result in junction to ambient temperature difference of 159°C/W x 0.48W = 76.32°C, thereby allowing operation up to an ambient temperature of 73.68°C for the absolute maximum junction temperature of 150°C.

Supertex, Inc. 1235 Bordeaux Drive, Sunnyvale, CA 94089 TEL: (408) 222-8888 FAX: (408) 222-4895 www.supertex.com

Design Information - *continued*

Operating from a full wave rectified AC input

For these applications there is no minimum input voltage, thus adding a fixed value series resistor is not possible. However, a dynamic resistor consisting of a depletion MOSFET may be added as depicted in the following diagram.



This method limits the $+V_{IN}$ voltage to V_{DD} + $V_{GS(OFF)}$ of the depletion MOSFET for all input voltages and in fact raises the maximum allowable peak input voltage to the breakdown voltage rating of the depletion MOSFET. The worst-case power dissipation in the HV9906 is now given by the equation

$$\text{Power Dissipation HV9906} = (V_{DD} + V_{GS(OFF)max}) \times I_{IN}$$

and the dissipation in the depletion MOSFET is given by the equation

$$\text{Power Dissipation in MOSFET} \approx (V_S - V_{DD} - V_{GS(OFF)}) \times I_{IN}$$

Which for the previously calculated input current of 3mA, $265V_{RMS}$ input voltage and using the DN3145N8 depletion MOSFET yields the following results.

$$\text{Power Dissipation HV9906} = (11 + 3.5) \times 3 \times 10^{-3} = 43.5\text{mW}$$

$$\text{Power Dissipation in MOSFET} \approx (265 - 10 - 1.5) \times 3 \times 10^{-3}$$

$$\text{Power Dissipation in MOSFET} \approx 0.76\text{W}$$

Using High Thermal Conductivity Encapsulation

For an encapsulated application the required thermal resistance of the encapsulating material can be calculated using the following equation.

$$R_{\theta ca} = \frac{T_j - T_a - (R_{\theta jc} \times V_{IN(max)} \times I_{IN})}{V_{IN(max)} \times I_{IN}}$$

$R_{\theta ca}$ is the required thermal resistance of the encapsulating material.

T_j is the maximum junction temperature.

T_a is the maximum ambient temperature.

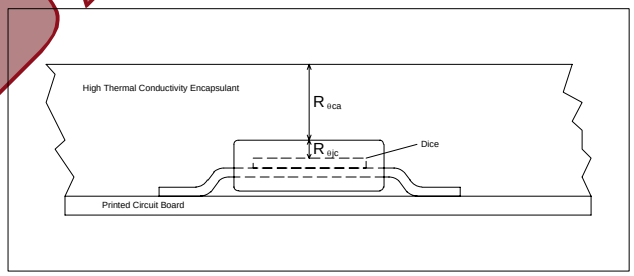
$R_{\theta jc}$ is the junction to case thermal resistance of the package.

$V_{IN(max)}$ is the maximum DC or RMS input voltage.

I_{IN} is the input current required at the highest operating frequency.

As an example, consider an application where the input current is 3mA as calculated earlier, operating with a maximum input voltage of $265V_{RMS}$ in an 85°C ambient and an SOIC packaged device will be used. The thermal resistance of the encapsulating material can then be calculated as follows.

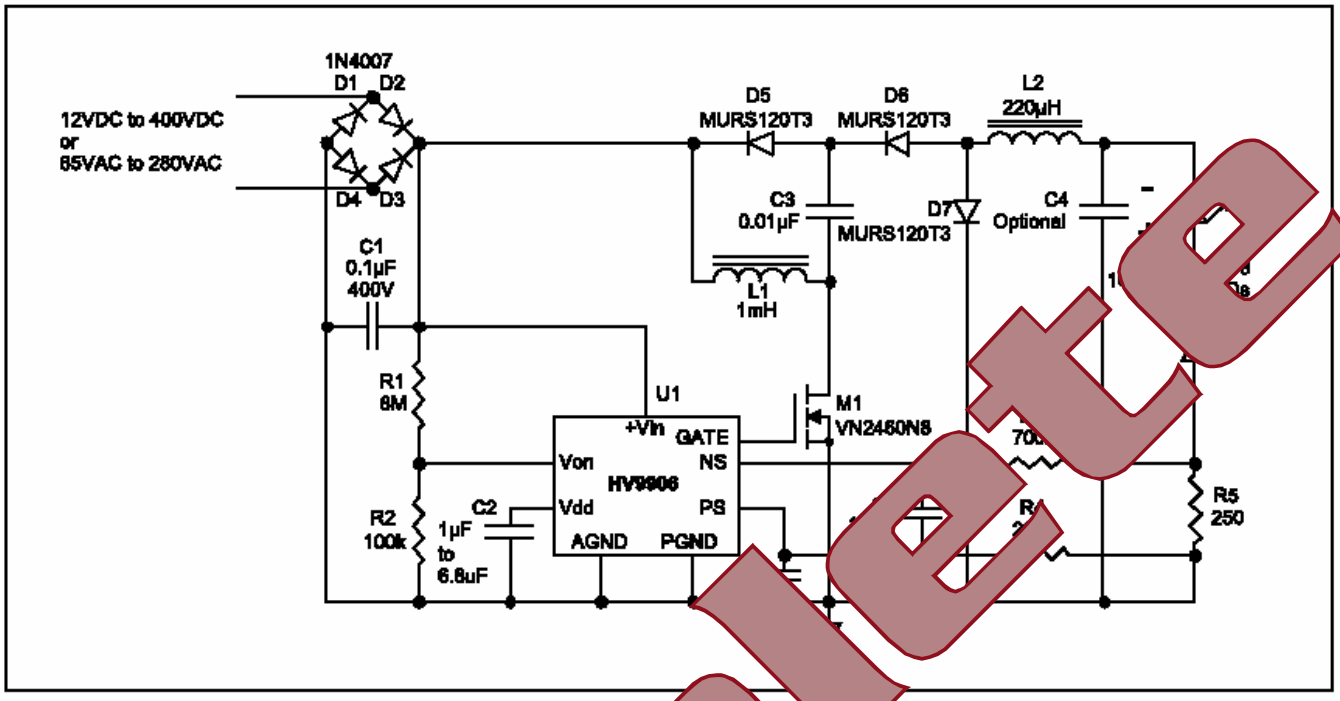
$$R_{\theta ca} = \frac{150 - 85 - (45 \times 265 \times 3 \times 10^{-3})}{265 \times 3 \times 10^{-3}} = 36.76°\text{C/W}$$



Supertex, Inc. 1235 Bordeaux Drive, Sunnyvale, CA 94089 TEL: (408) 222-8888 FAX: (408) 222-4895 www.supertex.com

Application Information

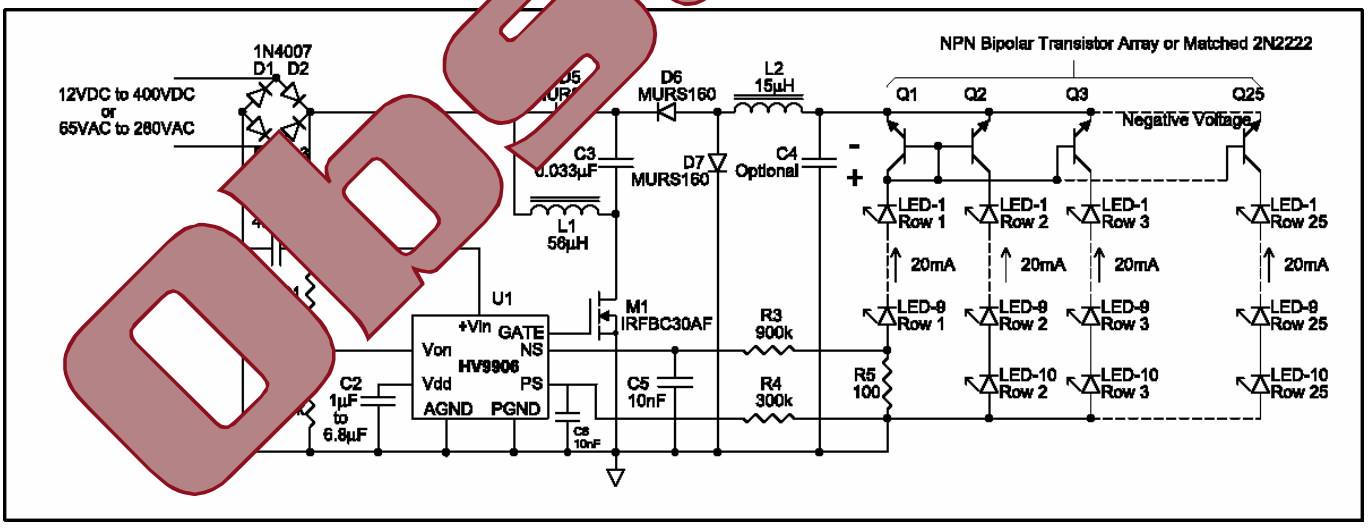
Universal Input Non-Isolated Constant 10mA Average Current LED Lamp Power Supply



This circuit provides a constant average current output, which may be used to power LED lamps. The circuit maintains a constant average current and the value of C4 capacitor controls the peak-t peak ripple, which decreases with increasing capacitor value.

s permissible then C4 may be omitted.

Universal Input Non-Isolated Constant 0.5A Averag nt LED Lamp Power Supply



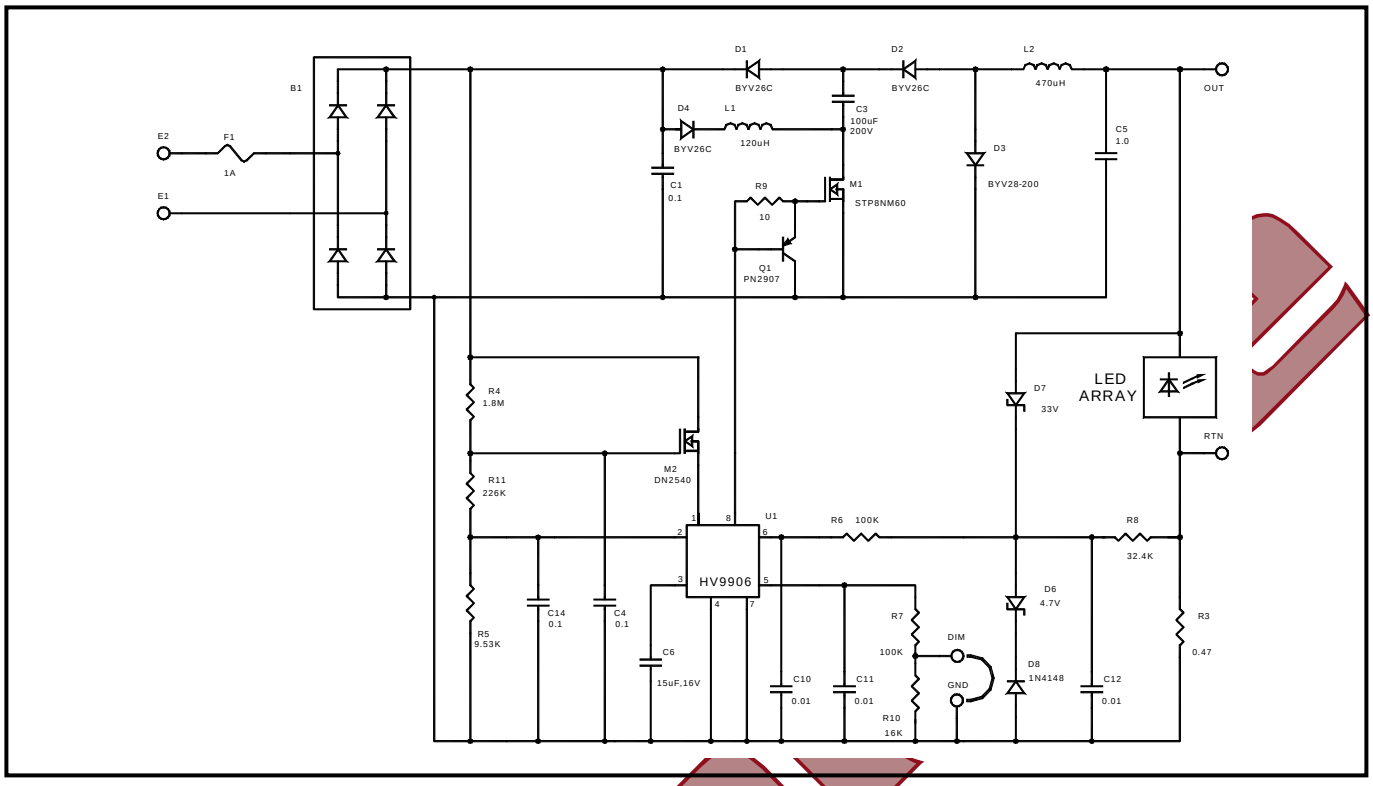
This circuit provides 0.5A constant average current output to power 249 LEDs , each operating at 20mA to form a large LED lamp or array. The circuit maintains a constant average current and the value of C4 capacitor controls the peak-to-peak ripple, which decreases with increasing capacitor value.

If current ripple is permissible then C4 may be omitted.

Supertex, Inc. 1235 Bordeaux Drive, Sunnyvale, CA 94089 TEL: (408) 222-8888 FAX: (408) 222-4895 www.supertex.com

Application Information - *continued*

Non-isolated Power Factor Corrected Constant Current LED Lamp Power Supply



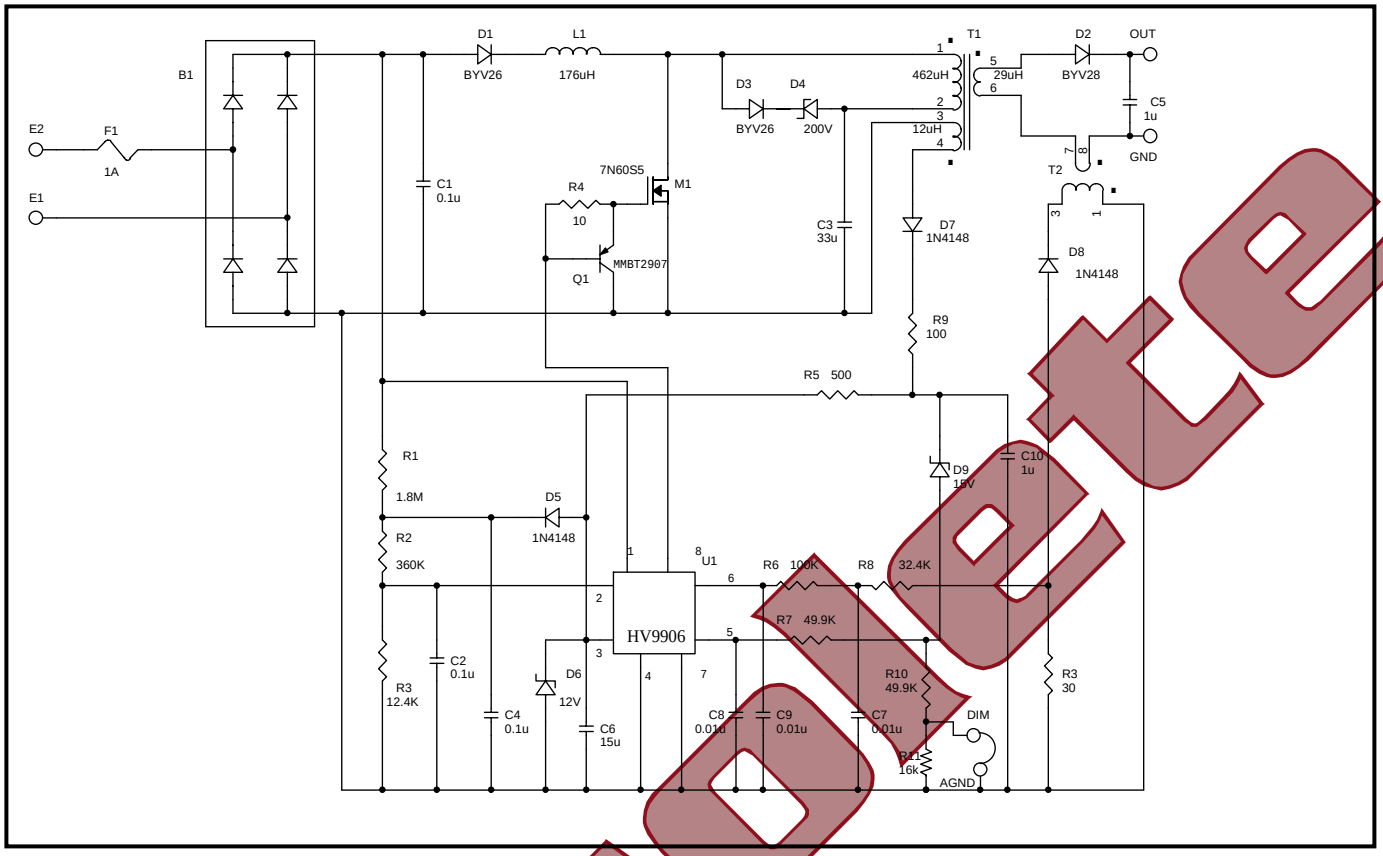
This power factor corrected circuit provides a constant non-isolated current output to power LED lamps. It is intended to meet the following specifications:

Input Voltage	80VAC to 135VAC
LED String Forward Voltage	30V max.
Power Factor	>0.95
THD	>15%
Output Current	700mA
Output Power	20W

Supertex, Inc. 1235 Bordeaux Drive, Sunnyvale, CA 94089 TEL: (408) 222-8888 FAX: (408) 222-4895 www.supertex.com

Application Information - *continued*

Isolated Power Factor Corrected Constant Current LED Lamp Power Supply



This power factor corrected circuit provides a constant isolated current output to power LED lamps. It is intended to meet the following specifications:

Input Voltage	80VAC to 135VAC
LED String Forward Voltage	21-23V
Power Factor	>0.95
THD	<20%
Output Current	750mA
Output Power	17W

Supertex, Inc. 1235 Bordeaux Drive, Sunnyvale, CA 94089 TEL: (408) 222-8888 FAX: (408) 222-4895 www.supertex.com